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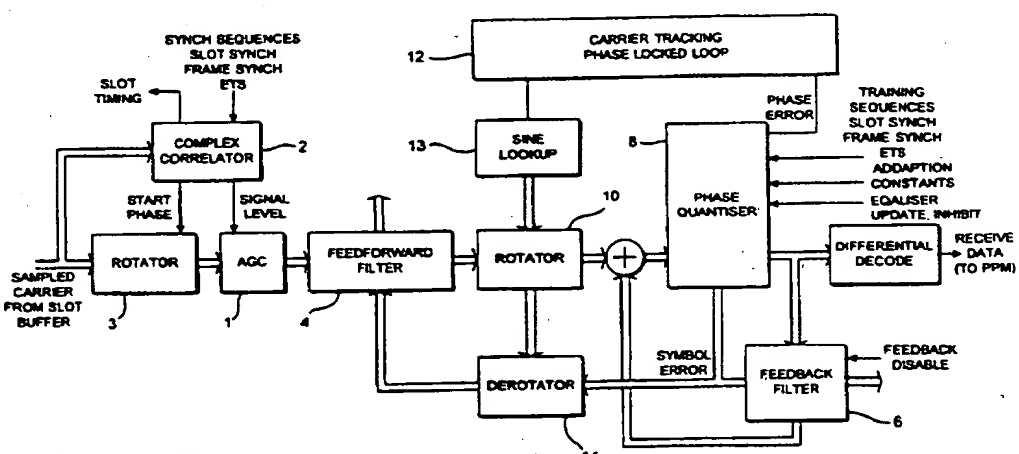

SYMBOL PROCESSOR FUNCTIONAL BLOCK DIAGRAM

(57) Abstract

A demodulator for a receiver of digital data messages sent in predetermined time slots within fixed length time frames includes an adaptive filter operative on each received data packet to determine digital bit values and to adapt filter coefficients. Filter coefficient values upon filtering a data packet in a time slot are used as initial values in adaptive filtering the next received data packet in the corresponding time slot of the next frame.

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ADAPTIVE FILTER FOR USE IN A TDM/TDMA RECEIVER

The present invention relates to a demodulator for a receiver of digital data messages sent in predetermined time slots within fixed length time frames.

Numerous equaliser adaption (i.e. adaptive digital filtering) methods have been developed and widely applied. The most widely reported are known as Least Mean Squares (LMS) and Recursive Least Squares (RLS) algorithms. The fundamental difference between the two types is the error minimisation criterion used to adjust the filter coefficients. As its name suggests, LMS minimises the statistical expectation value (mean) of the error and theoretically only converges to an optimal solution after an infinite number of iterations. By contrast, RLS minimises the instantaneous error for a given set of operating parameters and has convergence properties dictated only by the data it is given to process. The emergence of these two method types can be attributed to their relative advantages and disadvantages:

> LMS is comparatively slow to converge, making it poor at tracking moderate to fast channel variations, but is efficient to implement.

> RLS converges rapidly, has good tracking properties but has a high computational cost and susceptibility to instability.

Over the years, both "Fast" and compromise variants of the basic RLS algorithms have been developed in an attempt to reduce its computational requirements but these are still 5 to 10

times more computationally intensive than LMS. A detailed coverage of LMS, RLS and adaptive techniques generally is given in the book "Adaptive Filter Theory" by Simon Haykin, Prentice Hall 1991 2nd Edition.

Adaptive filters (equalisers) are used in TDM/TDMA networks to compensate for multipath interference. Signals reflect from buildings, hills and high sided vehicles, and so can take various paths between a transmitter and receiver. As discussed in Cellular Radio Systems, DM Balston and RCV Macario Editors, Artech House Inc 1993, page 167 et seq., equalisation is undertaken by estimating the signal transfer properties of the transmission medium (eg. by determining impulse response) and then processing the received signal accordingly to compensate. There are several known methods for estimating the transfer function of the transmission path and most of these methods rely on receiving an expected data sequence. This is a training sequence sent as part of a data packet. The receiver detects the sequence and knowing what bit symbol pattern (1,0 etc), i.e. symbol, it is intended to represent, is able to estimate the transfer function most likely to have produced the received signal, and the filter (equaliser) coefficients required to compensate for the multipath distortion.

In known mobile TDM/TDMA networks, i.e. those having mobile subscribers, propagation delays can vary from frame-to-frame to such an extent that complete retraining of the equaliser is necessary before demodulation of each newly received data packet. Unfortunately, this means either that an RLS algorithm must be used at a high computational cost, or that a large number of training symbols must be incorporated in each data packet so as to enable retraining, with less other data being sent.

The invention is defined in the claims to which reference should now be made. Preferred features are laid out in the sub claims.

The present invention in its first aspect preferably provides a demodulator for a TDM/TDMA receiver unit including adaptive filter means operative on each received data packet in each time slot of a frame to determine digital bit values and to adapt filter coefficients, in which filter coefficients values upon filtering a data packet in a time slot are used as initial values in adaptive filtering the next received data packet in the corresponding time slot of the next frame. In the periods between corresponding time slots, filter coefficients are preferably stored in a memory for reuse.

Preferably, the demodulator includes correlation means operative to perform a complex correlation between received and expected synchronisation data to determine carrier phase at a predetermined symbol in the received packet. By "complex correlation" is meant correlation of data which includes values having both real and imaginary parts.

Such demodulators are particularly applicable in TDM/TDMA networks having base stations and subscriber units which substantially have fixed locations. Although fading effects due to multipath propagation might well occur, these effects change only slowly compared to the transmission frame rate. The preferred demodulator takes account of the expected slowly varying nature of multipath propagation by reusing filter coefficients adapted from previous frames. In consequence, the length of training sequences can be greatly reduced providing a larger proportion of the available bandwidth for user data.

In the preferred TDM/TDMA network which includes demodulators according to the present invention, data packets still include data sequences suitable for training, although the sequence is short. The preferred demodulator receives this expected sequence so as to determine the carrier phase and packet timing, but not necessarily for training the adaptive filter coefficients.

The preferred demodulator according to the present invention advantageously minimises the amount of training data required, thereby maximising the bandwidth available for user data and avoids the use of an RLS adaption algorithm. In consequence the preferred demodulator can be of simple construction and has low power consumption. Also, by using filter coefficients from the corresponding data packet of the previous frame as a starting point, a slowly converging and simple to implement filter coefficient adaption method can be used.

The present invention also relates to a method of adaptive filtering of each received data packet in each time slot of a frame to determine digital bit values and to adapt filter coefficients, in which filter coefficients values upon filtering a data packet in a time slot are used as initial values in adaptive filtering the next received data packet in the corresponding time slot of the next frame.

The present invention in its second aspect provides a demodulator preferably including correlation means operative to perform a complex correlation between received and expected synchronisation data to determine carrier phase at a predetermined symbol in the received packet. This has advantages of computational efficiency and speed of phase acquisition. The present invention also relates to a corresponding method to determine carrier phase in a

demodulator.

By way of example, reference will now be made to the accompanying drawings in which:

Figure 1 is a schematic diagram illustrating the system including a base station (BTE-Base Terminating Equipment) and subscriber unit (NTE - Network Terminating Equipment);

Figure 2 is a diagram illustrating frame structure and timing for a duplex link;

Figure 3 is a schematic diagram showing different types of data packet transmitted from a base station to a subscriber unit (i.e. downlink);

Figure 4 is a block diagram representing the symbol processor of the demodulator at a subscriber unit.

Figure 5 is a block diagram illustrating the correlator shown in Figure 4.

Figure 6 is a block diagram illustrating the rotator and Automatic Gain Control (AGC) shown in Figure 4, and

Figure 7 illustrates equaliser output quantisation according to a $\pi/4$ - Differential Quadrative Phase-Shift Keying Modulation Scheme.

The Basic System

As shown in Figure 1, the preferred system is part of a telephone system in which the local wired loop from exchange to subscriber has been replaced by a full duplex radio link between a fixed base station (BTE) and fixed subscriber unit (NTE). The preferred system includes the duplex radio link (Air Interface), and transmitters and receivers for implementing the necessary protocol. There are similarities between the preferred system and digital cellular mobile telephone systems such as GSM which are known in the art. This system uses a protocol based on a layered model, in particular the following layers: PHY (Physical), MAC (Medium Access Control), DLC (DataLink Control), NWK (Network).

One difference compared with GSM is that, in the preferred system, subscriber units are at fixed locations and there is no need for hand-off arrangements or other features relating to mobility. This means, for example, in the preferred system that directional antennae and mains electricity can be used.

Each base station in the preferred system provides six duplex radio links at twelve frequencies chosen from the overall frequency allocation, so as to minimize interference between base stations nearby. The frame structure and timing for a duplex link is illustrated in Figure 2. Each duplex radio link comprises an up-link from a subscriber unit to a base station and, at a frequency offset, a down-link from the base station to the subscriber unit. The down-links are TDM, and the up-links are TDMA. Modulation for all links is $\pi/4$ - DQPSK, and the basic frame structure for all links is ten slots per frame of 2560 bits, i.e. 256 bits per slot. The bit rate is 512kbps. Down-links are continuously transmitted and incorporate a broadcast

channel for essential system information. When there is no user information to be transmitted, the down-link transmissions continue to use the basic frame and slot structure and contain a suitable fill pattern.

For both up-link and down-link transmissions, there are two types of slot: normal slots which are used after call set-up, and pilot slots used during call set-up.

Each down-link normal slot comprises 24 bits of synchronisation information followed by 24 bits designated S-field which includes an 8 bit header followed by 160 bits designated D-field. This is followed by 24 bits of Forward Error Correction and an 8 bit tail, followed by 12 bits of the broadcast channel. The broadcast channel consists of segments in each of the slots of a frame which together form the down-link common signalling channel which is transmitted by the base station, and contains control messages containing link information such as slot lists, multi-frame and super-frame information, connectionless messages, and other information basic to the operation of the system.

During the call set-up, each down-link pilot slot contains frequency correction data and a training sequence for receiver initialisation, with only a short S- field and no D- field information.

Up-link slots basically contain two different types of data packet. The first type of packet, called a pilot packet, is used before a connection is set up, for example, for an ALOHA call request and to allow adaptive time alignment. The other type of data packet, called a normal packet, is used when a call has been established and is a larger data packet, due to the use

of adaptive time alignment.

Each up-link normal packet contains a data packet of 244 bits which is preceded and followed by a ramp of 4 bits duration. The ramps and the remaining bits left of the 256 bit slot provide a guard gap against interference from neighbouring slots due to timing errors. Each subscriber unit adjusts the timing of its slot transmissions to compensate for the time it takes signals to reach the base station. Each up-link normal data packet comprises 24 bits of synchronisation data followed by an S-field and D-field of the same number of bits as in each down-link normal slot.

Each up-link pilot slot contains a pilot data packet which is 192 bits long preceded and followed by 4 bit ramps defining an extended guard gap of 60 bits. This larger guard gap is necessary because there is no timing information available and without it the propagation delays would cause neighbouring slots to interfere. The pilot packet comprises 64 bits of sync followed by 104 bits of S-field which starts with an 8 bit header and finishes with a 16 bit Cyclic Redundancy Check, 2 reserved bits, 14 FEC bits, and 8 tail bits. There is no D-field.

The S-fields in the above mentioned data packets can be used for two types of signalling. The first type is MAC signalling (MS) and is used for signalling between the MAC layers of the base station and the MAC layer of a subscriber unit whereby timing is important. The second type is called associated signalling, which can be slow or fast and is used for signalling between the base station and subscriber units in the DLC or NWK layers.

The D-field is the largest data field. and in the case of normal telephony contains digitised speech samples. but can also contain non-speech data samples.

Provision is made in the preferred system for subscriber unit authentication using a challenge response protocol. General encryption is provided by combining the speech or data with a non-predictable sequence of cipher bits produced by a key stream generator which is synchronised to the transmitted super-frame number.

In addition. the transmitted signal is scrambled to remove dc components.

The subscriber unit demodulator is concerned with the physical reception of data transmitted in the direction base-to-subscriber (downlink).

There are currently three types of downlink packet. two of these are shown in Figure 3. From the demodulation perspective. the third packet type (Idle Packet) is the same as the Pilot Packet shown except that the DOWN-P-DATA data field is replaced with a fixed fill pattern.

The Subscriber Unit Demodulator

The following functions are undertaken by a sub-section of the subscriber unit demodulator apparatus known as the Symbol Processor:

Synch Correlation (synch detection. slot timing recovery, initial carrier phase recovery),

Digital AGC,

Equalisation,

Carrier phase Tracking, and

Slicing (symbol decisions).

The Symbol Processor operates as one of a basic (non-equalising) coherent receiver, a linear equaliser, or a decision feedback equaliser (DFE). Which is best for any particular subscriber unit will be governed by characteristics of the RF propagation path. The basic receiver is likely to perform best where multipath effects are not significant, the linear equaliser will offer a performance benefit where multipath interference is present but not severe and the DFE has the potential to operate through severely dispersive channels.

Symbol Processing

The functions performed by the Symbol Processor are shown in Figure 4 which is a signal flow diagram in which double-edged arrows denote paths for complex data.

The output signal from the radio frequency (RF) section (not shown) of the subscriber receiver is digitised and presented to the symbol processor at baseband as a sequence of complex samples. These samples are buffered to enable non-real-time processing. The demodulated (output) bit sequence which can be a normal or pilot packet or a Broadcast data fragment, depending upon operating mode, is passed to a separate circuit block responsible for deformatting and bit-level protocol processing.

With the exception of the correlator 2, which operates at the input sample rate, all processing is performed iteratively at symbol rate. Timing is organised such that the received Slot Synch sequence of the captured packet falls within a predetermined region of the input buffer used by the correlator 2.

Complex Correlation

Complex correlation in correlator 2 with a stored representation of the expected synch sequence (Slot Synch or Frame Synch) then produces estimates of instantaneous carrier phase and signal level (gain) which are subsequently used to scale, and phase-align (ie. rotate), the input data samples. Rotation is undertaken by rotator 3, to establish the carrier phase mid-way through the synch sequence and having a zero degree reference defined by the stored synch pattern. Scaling is undertaken by operation of Automatic Gain Control (AGC) circuitry 1.

The expected synch sequences (Slot Synch in slots 1 to 9, Frame Synch in slot 0) are each stored as two sequences of N samples, one sequence being the real components, ReY [n] as shown in Figure 5, and the other sequence being the imaginary components, ImY [n] shown in Figure 5. The sequence Y [n] represents the expected constellation points produced by optimally sampling a baseband carrier signal which has been Π/4 - DQPSK modulated with a binary Slot Synch or Frame Synch sequence, and filtered through a matched receiving filter.

The stored sequences Y [n] are stored either as hardwired constants or preferably programmed into static registers 16.

The correlator 2 processes one sample per symbol from a shift register 18 which holds input data X [n] from the slot buffer (not shown), real and imaginary components ReX [n] and ImX [n] being held separately. The static registers 16 hold the expected values Y [n]. The shift register 18 is updated once per input sample and effectively holds decimated sequences from the synch window (see later), for example sample 1, 3, 5, 7 in the case of two samples per symbol.

As shown in Figure 5, the correlator consists of two main functional blocks. One block 20 undertakes sum-of products calculations on the real component of the input data ReX [n]. The other block 22 undertakes sum of products calculations on the imaginary component of the input data ImX [n]. The respective real and imaginary output signals 24, 26 from the sum-of-products circuits 20, 22 are combined in respective adders 28, 30 to provide real and imaginary components ReRxy, ImRxy of a discrete cross-correlation function Rxy [n].

The received Synch sequence is known to occupy a certain region of the slot buffer upon reception of a packet. Cross correlation is performed across a limited region of the slot buffer (synch window) which is known to contain the incoming Synch pattern. For each element of the correlation function, the output power is evaluated by squaring in squarers 32, 34 and adding in adder 36. A power peak is detected by peak detector 38 when the expected sequence Y [n] and the incoming decimated synch sequence are time aligned. The detector then outputs a peak signal Rxy (peak) which is independent of incoming carrier phase. The reciprocal of the peak power value Rxy (peak) is determined and output as a scale factor applied to the AGC circuitry 1 as shown in Figure 6. Upon the peak being detected, adders 28, 30 provide real and imaginary peak power components Re Rxy (peak) and Im Rxy (peak)

which are applied as phase correction signals to the rotator 3 as shown in Figure 6.

As illustrated in Figure 6, in the rotator 3, real and imaginary components of input data samples, ReX [n] and ImX [n] are respectively multiplied by the real and imaginary peak power values Re Rxy (peak) and Im Rxy (peak). The resulting real and imaginary products are summed to give phase corrected output signals 42, 44. These output signals 42, 44 are applied to the AGC circuitry 1 for scaling by the scale factor before being output as phase and gain corrected samples ReX [n]' and ImX [n]'.

Demodulation

The phase and gain-corrected samples, starting with the one closest to the middle of synch, are applied to the main demodulation loop which carries out:

. symbol slicing (absolute phase decoding);

carrier tracking (phase locked loop);

multipath equalisation.

The equaliser is implemented in four principal sections:

a feedforward filter 2

a feedback filter 4

a quantiser 8 and a

filter adaption mechanism

The two filter sections each consist of a complex tapped delay line (ie. a Finite Impulse Response filter) with variable tap weights (ie. coefficients).

The feedforward filter 4, which has at least one delay element/coefficient per symbol period, takes input data from the AGC block 1, convolves the samples held in its tapped delay line with the current coefficient set and presents its output to the rotator 10 of the phase locked loop (PLL) 12.

Likewise, the feedback filter 4, which has only one delay element/coefficient per symbol period, convolves constellation decisions from the quantiser 8 with a further coefficient set. The combined output from feedforward and feedback filters 4, 6 constitutes the equaliser output and this particular configuration of filter sections is generally referred to as a decision feedback equaliser (DFE).

In operation, the equaliser generates one (equalised) output sample per symbol period which is fed to the quantiser 8. The function of the quantiser 8 is then to compare the output with the set of 'ideal' constellation points characterising the modulation scheme and to select the constellation point which is closest in the Euclidean sense. This process is depicted for the $\pi/4$ - DQPSK modulation scheme in Figure 7 which shows an equaliser output sample X being selected as having a closest constellation point Y' of possible constellation points Y.

The selected constellation point Y' forms the quantiser 8 decision for the current receive symbol and, as such, the next input sample for the feedback filter 4. Successive quantiser 8 decisions are also fed to a symbol decoding circuit where they are processed to recover the

transmitted bit sequences.

The difference between the equaliser output X and the selected constellation point Y represents the decision error Z for the current symbol and this is used by the coefficient adaption mechanism to drive the long term error to zero. The equaliser is said to have converged when the coefficients in the feedforward and feedback filters 4, 6 have reached values which adequately mitigate the effects of intersymbol interference.

Equaliser coefficients are initialised with constants (zeroes except for the 'main tap' which is set to unity) prior to pilot packet processing (the extended training sequence ETS is used to train the equaliser initially). Thereafter, the final values in one slot are used as the starting values in the corresponding slot of the next frame.

The two filter outputs are combined on the quantiser side of a phase rotator 10 which is driven by a decision-directed phase locked loop 12. Slicing produces a phase error term and, by subtracting the rotator output vector from the closest candidate constellation point, a symbol error vector suitable for equaliser coefficient updating.

The phase error term is passed to the carrier tracking algorithm which modifies the current phase estimate in preparation for the next symbol. A sine lookup table 13 is used to convert the phase estimate to an equivalent cartesian representation. At the start of each packet, or more specifically for the first sample to be processed, which is the middle sample in the synch sequence, the phase reference (a state variable within the carrier tracking algorithm) is set to zero. Thereafter it is adapted by means of a dedicated carrier tracking algorithm.

Two representations of the symbol error vector are required: the unprocessed error for feedback updates and a 'derotated' error vector, which reintroduces the phase offset removed by the phase locked loop, for feedforward updates. Derotation by derotator 14 is necessary to re-establish the correlative relationship between the decision error and samples in the feedforward filter. Coefficients are adjusted using the so-called Stochastic Gradient LMS algorithm although any direct-form adaption algorithm could be employed.

The adaption properties of the carrier tracking loop and equaliser are chosen to ensure that carrier phase variations (including frequency offset) are removed by the actions of the phase-locked loop leaving the equaliser to compensate exclusively for multipath channel variations.

On completing slot demodulation, the equaliser coefficients are stored away for use in the corresponding slot of the following frame.

The operation of the present invention will now be related to the steps involved in normal and pilot packet processing. To process a pilot packet, the following steps are involved:

1) Digitise and capture the required pilot packet into the slot buffer (in the preferred demodulator synch processing and packet capture are overlapped to minimise group delay).

2) Restore the equaliser coefficients to their values at the end of the preceding slot, one frame earlier. (For the first pilot packet, the coefficients are initialised with constant data).

3) Correlate for Slot Synch data (ie. Frame Synch in slot 0) over the synch window. use the peak output of the correlator to scale and rotate all samples in the synch region of the slot buffer. This aligns the phase of the input carrier with the equaliser coefficients.

4) Pass the scaled and rotated input Synch samples through the demodulator/equaliser, adapting the equaliser coefficients and local phase reference based upon the known symbol (Synch) sequence.

5) Demodulate the Synch sequence to provide an indication of packet integrity. A synch sequence received in error may be used, for example, to inhibit equaliser adaption thereby preventing potential corruption.

6) Correlate for the extended training sequence ETS over a delayed synch window. Use the peak correlator output to scale and rotate the samples in the ETS and DOWN-P-DATA regions of the slot buffer. This aligns the phase of the input carrier with the equaliser coefficients.

7) Determine the peak offset from the nominal synch position and, if necessary, realign the demodulator time frame to compensate.

8) Reset the local phase reference (to 0 degrees) and then pass the scaled and rotated ETS samples through the demodulator/equaliser, adapting the equaliser coefficients and phase reference based upon the known (ETS) sequence. This is the normal

training procedure.

9) Pass the (scaled and rotated) DOWN-P-DATA samples through the demodulator/equaliser, adapting the equaliser coefficients and phase reference based upon constellation decisions. This is typically a decision-directed adaption. The demodulated DOWN-P-DATA contribution is passed on for bit-level protocol processing.

10) Store away the equaliser coefficients for the next pilot or normal packet on this carrier (ie. in the next frame).

A switch to normal packet reception occurs once the equaliser has successfully trained from pilot packets. The preferred procedure for normal packet reception is then as follows:

1) Digitise and capture the required normal packet into the slot buffer (in the preferred demodulator synch processing and packet capture are overlapped to minimise group delay).

2) Restore the equaliser coefficients to their values at the end of the preceding slot, one frame earlier. (For the first normal packet, the coefficients are established during pilot training).

3) Correlate for Slot Synch (Frame Synch in slot 0) over the synch window. Use the peak correlator output to scale and rotate all samples in the slot buffer. This aligns

the phase of the input carrier with the equaliser coefficients.

4) Pass the scaled and rotated input Synch samples through the demodulator/equaliser, adapting the equaliser coefficients and local phase reference based upon the known symbol (Synch) sequence. Demodulate the Synch sequence to provide an indication of packet integrity. A synch sequence received in error may be used, for example, to inhibit equaliser adaption thereby preventing potential corruption.

5) Pass the (scaled and rotated) DOWN-N-DATA samples through the demodulator/equaliser. adapting the equaliser coefficients and phase reference based upon constellation decisions. This is typically referred to a decision-directed adaption. The demodulated DOWN-N-DATA is passed on for bit-level protocol processing.

6) Store away the equaliser coefficients for the next pilot or normal packet on this carrier (ie. in the next frame).

CLAIMS

1. A demodulator for a receiver of digital data messages sent in predetermined time slots within fixed length time frames, the demodulator including adaptive filter means operative on each received data packet in each time slot of a frame to determine digital bit values and to adapt filter coefficients, in which values of filter coefficients upon filtering a data packet in a time slot are used as initial values in adaptive filtering the next received data packet in the corresponding time slot of the next frame.

2. A demodulator for a receiver of digital data messages sent in predetermined time slots within fixed length time frames according to claim 1, in which in the periods between corresponding time slots, filter coefficients are stored in a memory for reuse.

3. A demodulator for a receiver of digital data messages sent in predetermined time slots within fixed length time frames according to claim 2, in which the demodulator includes correlation means operative to perform a complex correlation between received and expected synchronisation data to determine carrier phase at a predetermined symbol in the received packet.

4. A demodulator for a receiver of digital data messages according to claim 3, in which the received synchronisation data is selected upon reception as that being at a predetermined position or positions within the received data packet.

5. A demodulator for a receiver of digital data messages according to claim 3 or claim 4, in which the determined carrier phase is used to correct phases determined for other

received data.

6. A receiver of digital data messages sent in predetermined time slots within fixed length time frames comprising a demodulator according to any preceding claim.

7. A receiver according to claim 6, which is a subscriber unit operative to receive time division multiplex (TDM) data signals.

8. A receiver according to claim 7, which is a subscriber unit having a fixed location.

9. A receiver according to claim 6, which is a base station operative to receive time division multiple access (TDMA) data signals.

10. A receiver according to any of claims 6 to 9, operative to receive digital data messages sent by radio.

11. Communications means comprising a plurality of subscriber units each operative to receive digital data messages comprising data packets in predetermined time slots within fixed length time frames from a base station, and the base station operative to receive digital data messages comprising data packets in predetermined time slots within fixed length time frames from the subscriber units, the base station and subscriber units each comprising a receiver including a demodulator, the demodulators each including adaptive filter means operative on each received data packet in each time slot of a frame to determine digital bit values and to adapt filter coefficients, in which values of filter coefficients upon filtering a data packet in

a time slot are used as initial values in adaptive filtering the next received data packet in the corresponding time slot of the next frame.

12. A method of demodulating a digital data message received as data packets in predetermined time slots within fixed length time frames including adaptive filtering of each received data packet to determine digital bit values and to adapt filter coefficients, in which filter coefficients values upon filtering a data packet in a time slot are used as initial values in adaptive filtering the next received data packet in the corresponding time slot of the next frame.

13. A demodulator of digital data messages received as data packets in time slots within fixed length time frames including correlation means operative to perform a complex correlation between received and expected synchronisation data to determine carrier phase at a predetermined symbol in a received data packet.

14. A demodulator of digital data messages according to claim 13, in which the received synchronisation data is selected upon reception as that being at a predetermined position or positions within the received data packet.

15. A demodulator of digital data messages according to claim 13 or claim 14, in which the received data packet is stored in a memory for processing.

16. A demodulator of digital data messages according to any of claims 13 to 15, in which the correlation means comprises first means and second means, the first means being

operative to determine sum of product values for real components of received synchronisation data multiplied by corresponding real and imaginary components of expected synchronisation data, the second means being operative to determine sum of product values for imaginary components of the received synchronisation data multiplied by real and imaginary components of the expected synchronisation data, the respective real and imaginary output signals from the first means and second means being combined by combination means to provide real and imaginary cross correlation function components, the correlation means comprising squaring means operative to provide values proportional to the respective real and imaginary cross correlation function components squared and detector means operative to detect a power peak, the combination means providing the real and imaginary cross correlation function components at which the power peak occurs as the real and imaginary components of the carrier phase.

17. A demodulator of digital data messages according to claim 16, in which the real and imaginary cross correlation function components at which the power peak occurs are used for gain control.

18. A demodulator of digital data messages according to any of claims 13 to 17, in which values determined as real and imaginary components of the carrier phase are applied as phase correction signals in subsequent demodulation of received data.

19. A method of determining carrier phase in a demodulator of digital data received as data packets in time slots within fixed length time frames by performing a complex correlation between received and expected synchronisation data to determine carrier phase at

a predetermined symbol in a received data packet.

FIG. 1

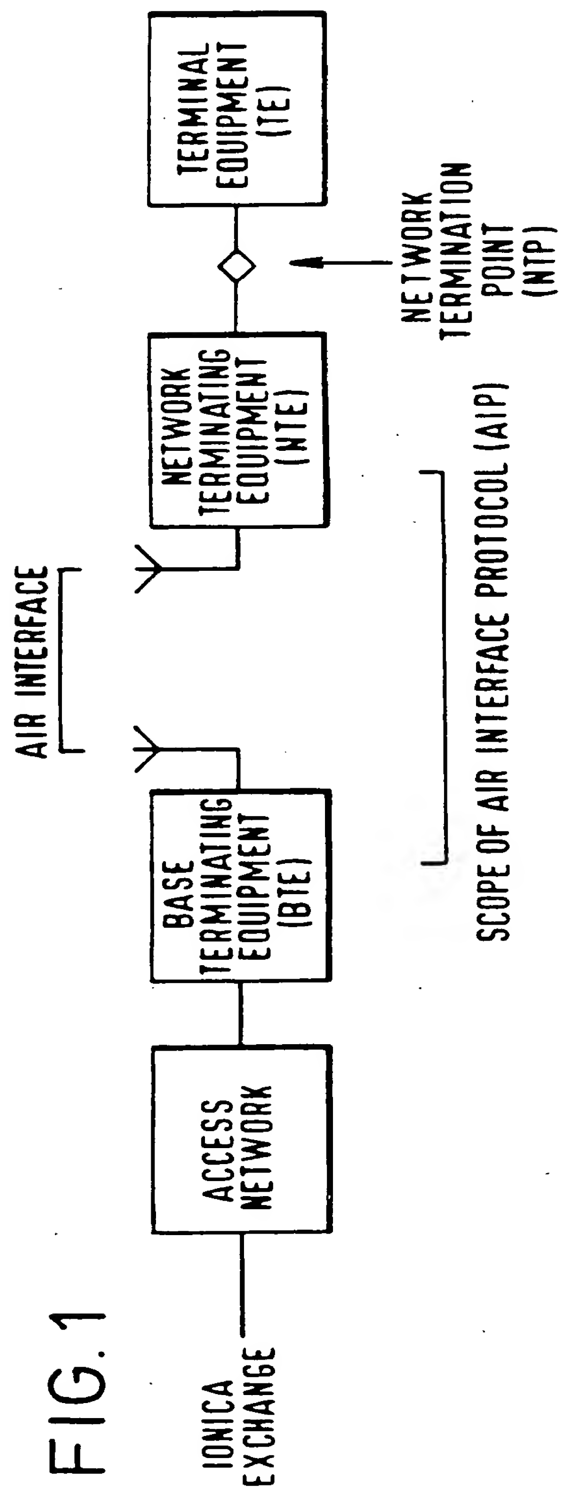
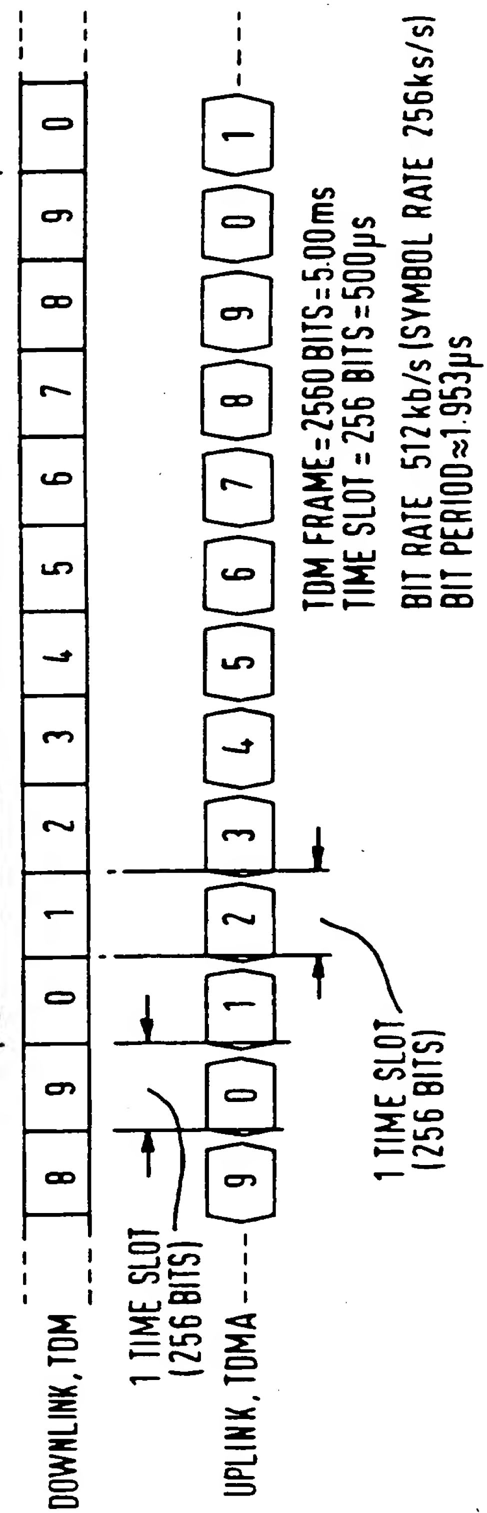

IONICA EXCHANGE
ACCESS NETWORK
BASE TERMINATING EQUIPMENT (BTE)
AIR INTERFACE
NETWORK TERMINATING EQUIPMENT (NTE)
NETWORK TERMINATION POINT (NTP)
TERMINAL EQUIPMENT (TE)
SCOPE OF AIR INTERFACE PROTOCOL (AIP)

FIG. 2


DOWNLINK, TDM
UPLINK, TDMA
1 TIME SLOT (256 BITS)
TDM FRAME (2560 BITS)
8 9 0 1 2 3 4 5 6 7 8 9 0
9 0 1 2 3 4 5 6 7 8 9 0 1
1 TIME SLOT (256 BITS)
TDM FRAME=2560 BITS=5.00ms
TIME SLOT = 256 BITS =500μs
BIT RATE 512kb/s (SYMBOL RATE 256ks/s)
BIT PERIOD≈1.953μs

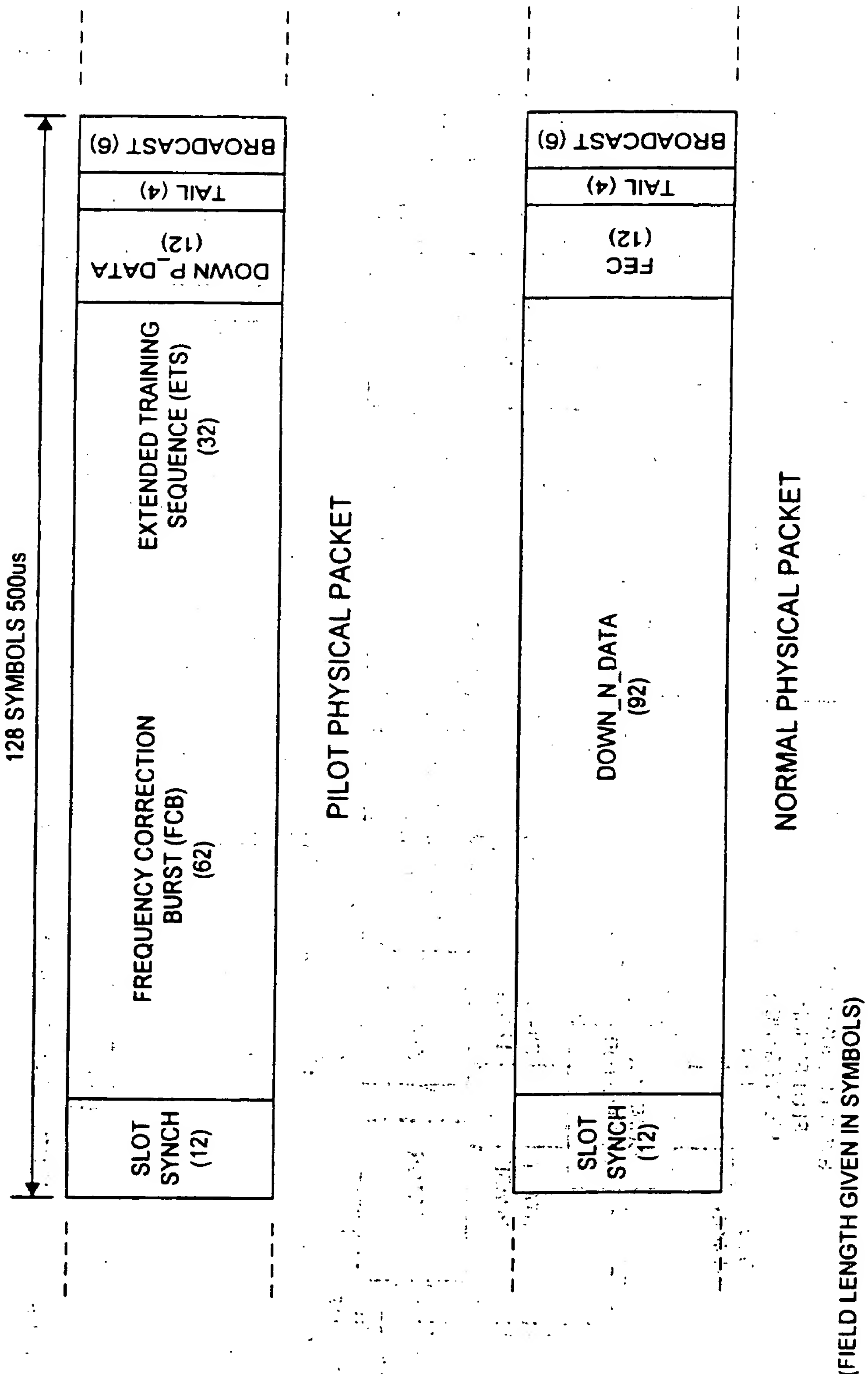


FIG. 3
DOWNLINK PHYSICAL PACKET STRUCTURES

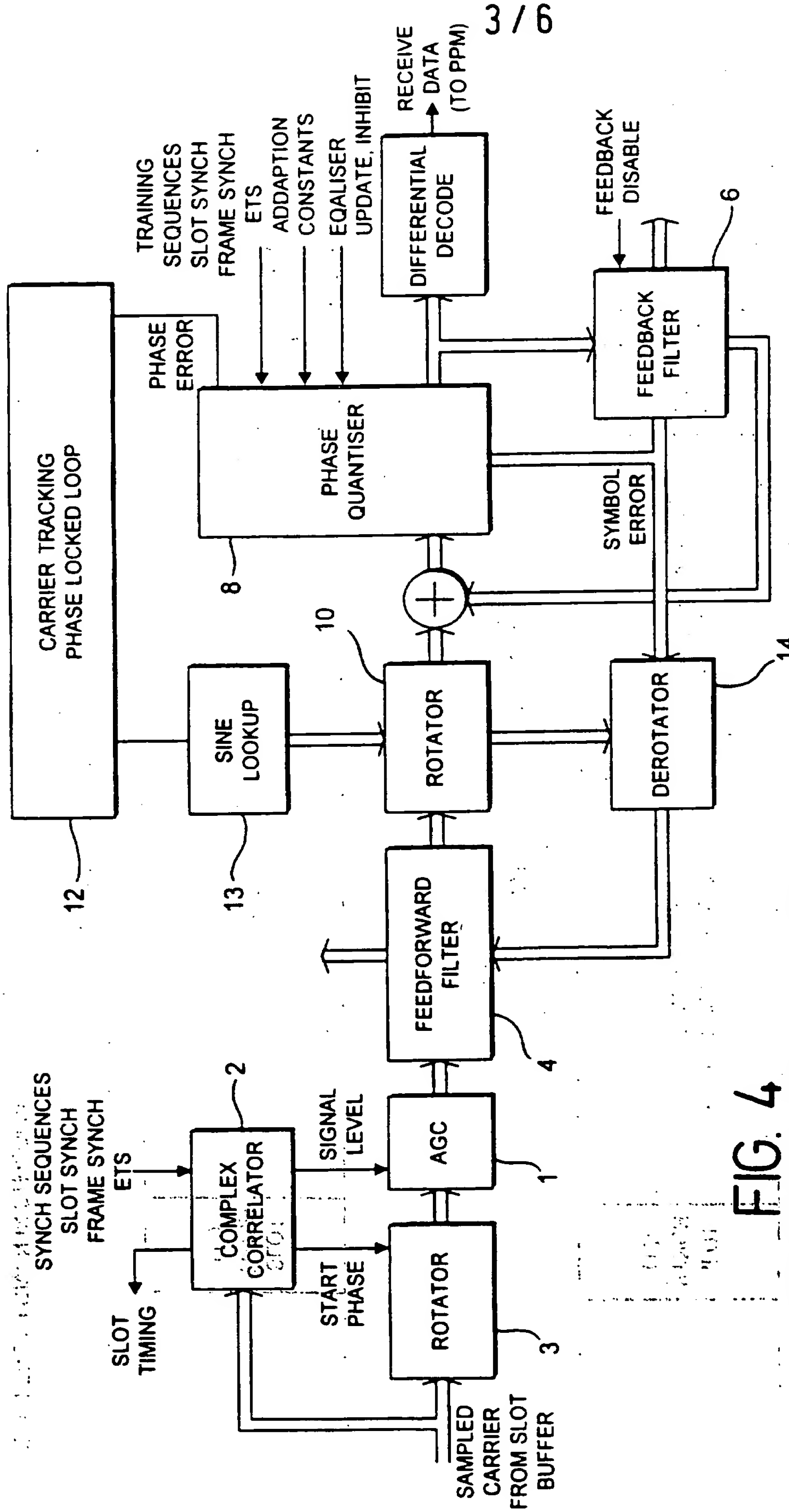
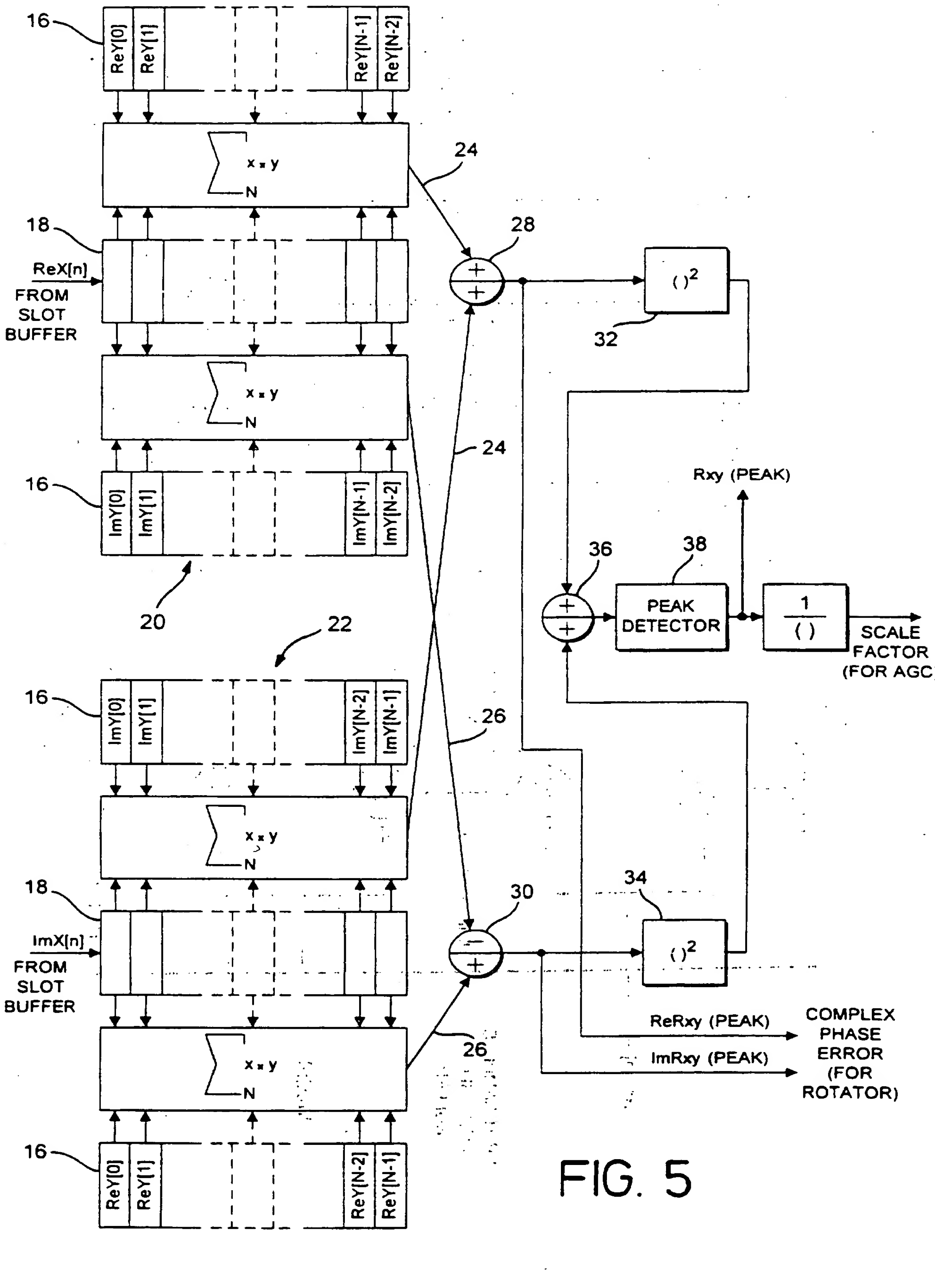


FIG. 4

SYMBOL PROCESSOR FUNCTIONAL BLOCK DIAGRAM



16
ReY[0]
ReY[1]
ReY[N-1]
ReY[N-2]
x * y
N
24
18
ReX[n]
FROM SLOT BUFFER
28
( )²
32
24
16
ImY[0]
ImY[1]
ImY[N-1]
ImY[N-2]
Rxy (PEAK)
36
38
PEAK DETECTOR
1/( )
SCALE FACTOR (FOR AGC)
20
22
16
ImY[N-2]
ImY[N-1]
26
18
ImX[n]
FROM SLOT BUFFER
30
34
ReRxy (PEAK)
ImRxy (PEAK)
COMPLEX PHASE ERROR (FOR ROTATOR)
26
16
ReY[N-2]
ReY[N-1]

FIG. 5

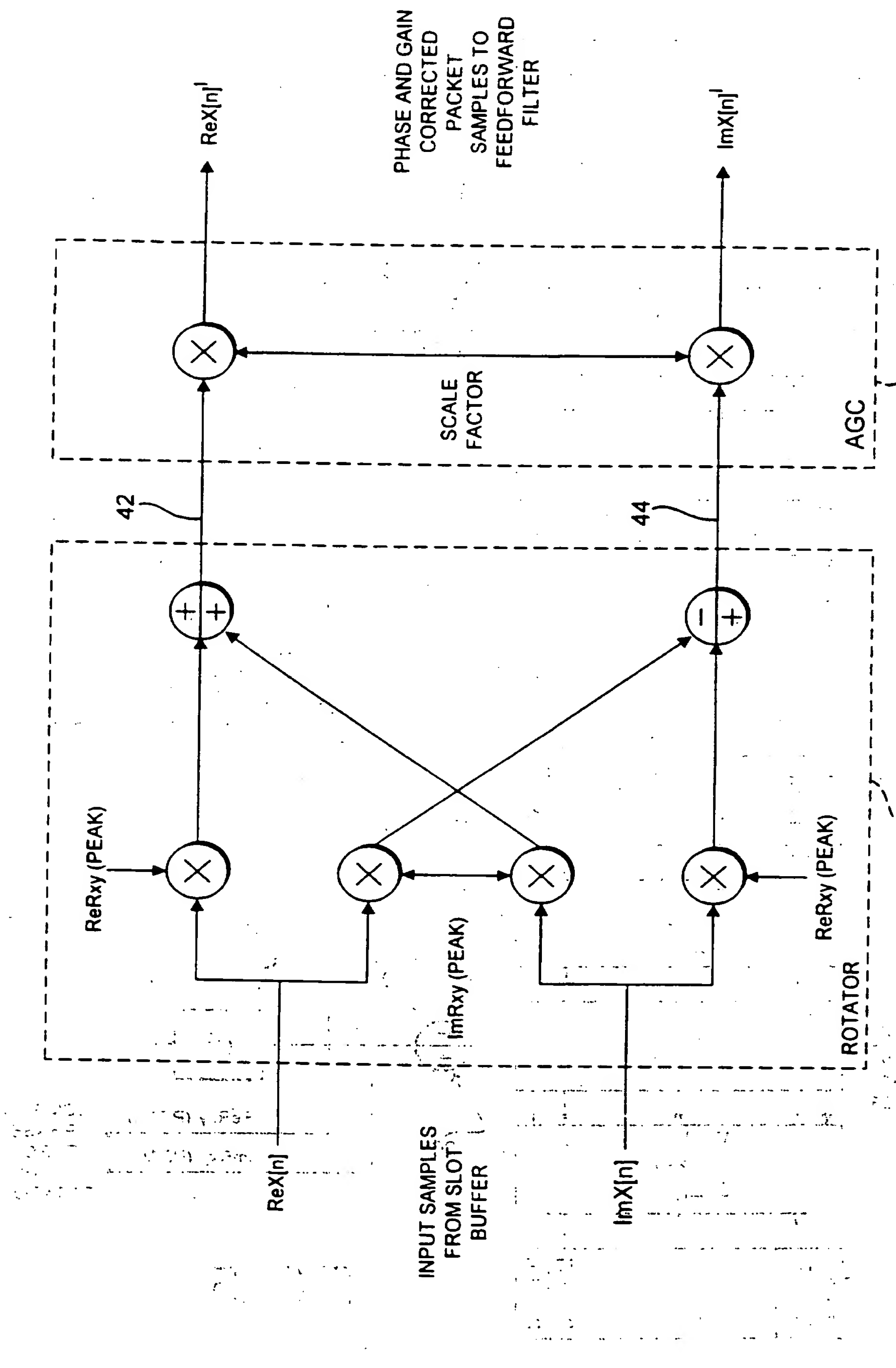

PHASE AND GAIN CORRECTED PACKET SAMPLES TO FEEDFORWARD FILTER
ReX[n]'
ImX[n]'
SCALE FACTOR
AGC
1
42
44
ReRxy (PEAK)
ImRxy (PEAK)
ReRxy (PEAK)
ROTATOR
3
ReX[n]
INPUT SAMPLES FROM SLOT BUFFER
ImX[n]

FIG. 6

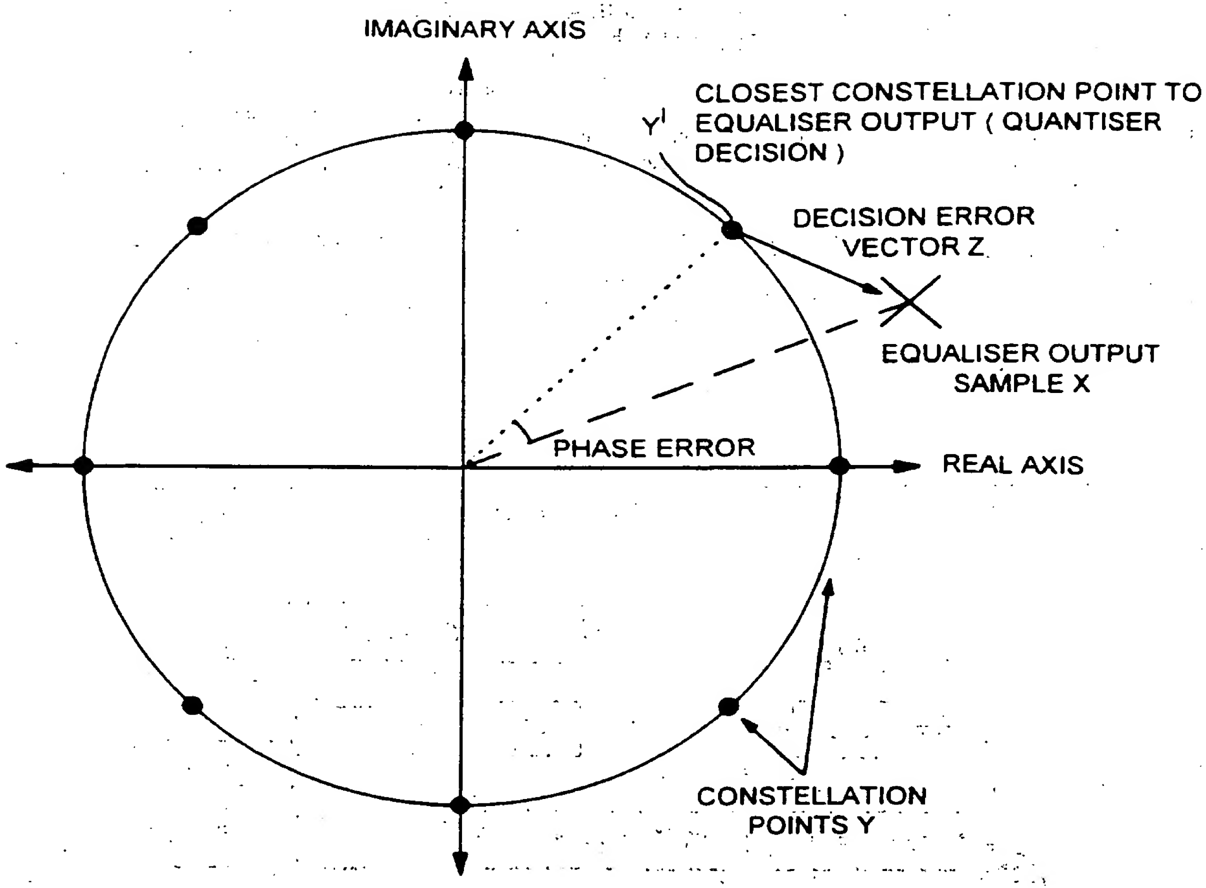

IMAGINARY AXIS
CLOSEST CONSTELLATION POINT TO EQUALISER OUTPUT (QUANTISER DECISION)
Y'
DECISION ERROR VECTOR Z
EQUALISER OUTPUT SAMPLE X
PHASE ERROR
REAL AXIS
CONSTELLATION POINTS Y

FIG. 7

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International Bureau

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(71) Applicant (*for all designated States except US*): IONICA INTERNATIONAL LIMITED [GB/GB]; Cowley Road, Cambridge CB4 4AS (GB).

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(75) Inventor/Applicant (*for US only*): RUDKIN, Paul, William [GB/GB]; 12 Tamarin Gardens, Cherry Hinton, Cambridge CB1 4BH (GB).

(74) Agent: SARUP, David, Alexander; Withers & Rogers, 4 Dyer's Buildings, Holborn, London EC1N 2JT (GB).

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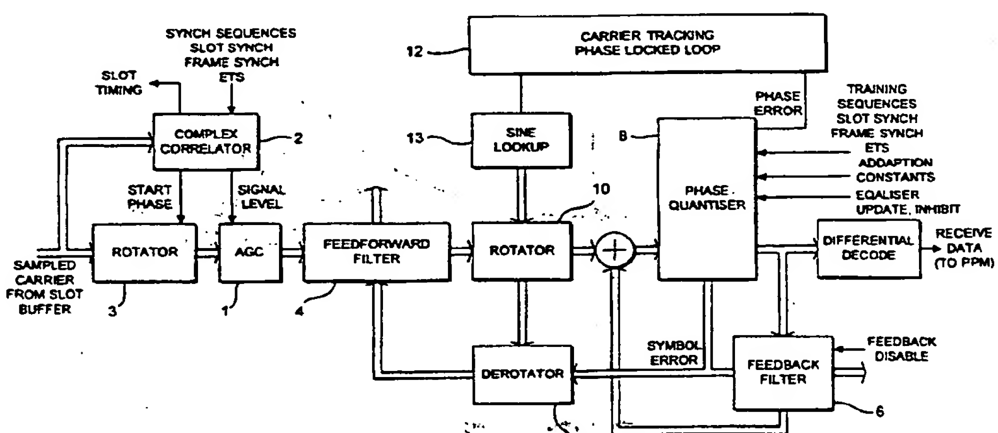
(54) Title: ADAPTIVE FILTER FOR USE IN A TDM/TDMA RECEIVER



SYMBOL PROCESSOR FUNCTIONAL BLOCK DIAGRAM

(57) Abstract

A demodulator for a receiver of digital data messages sent in predetermined time slots within fixed length time frames includes an adaptive filter operative on each received data packet to determine digital bit values and to adapt filter coefficients. Filter coefficient values upon filtering a data packet in a time slot are used as initial values in adaptive filtering the next received data packet in the corresponding time slot of the next frame.

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INTERNATIONAL SEARCH REPORT

International Application No
PCT/GB 96/00947

A. CLASSIFICATION OF SUBJECT MATTER
IPC 6 H04L25/03 H04L27/233

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 6 H04L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X Y	PATENT ABSTRACTS OF JAPAN vol. 014, no. 455 (E-0985), 28 September 1990 & JP,A,02 183614 (MATSUSHITA), 18 July 1990, see abstract ---	1,2,6-12 3-5
X Y	EP,A,0 106 136 (COMMUNICATIONS SATELLITE CORP.) 25 April 1984 see page 7, line 5 - page 8, line 2 see page 10, line 35 - page 11, line 7 ---	1,2,6-12 3-5
X Y	EP,A,0 639 914 (MARTIN MARIETTA CORP.) 22 February 1995 see page 4, line 31 - line 33 see page 5, line 29 - page 7, line 1 see figures 2,3 --- -/--	13-19 3-5

[X] Further documents are listed in the continuation of box C.

[X] Patent family members are listed in annex.

* Special categories of cited documents :

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"&" document member of the same patent family

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Date of the actual completion of the international search	Date of mailing of the international search report
11 October 1996	18. 10. 96
Name and mailing address of the ISA European Patent Office, P.B. 5818 Patentlaan 2 NL - 2280 HV Rijswijk Tel. (+31-70) 340-2040, Tx. 31 651 epo nl, Fax (+31-70) 340-3016	Authorized officer Ghigliotti, L

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C.(Continuation) DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US,A,4 583 048 (GUMACOS CONSTANTINE ET AL.) 15 April 1986 see column 6, line 9 - column 8, line 57	13-19
Y	see figure 3	3-5
X	US,A,4 238 739 (ANDREN CARL F. ET AL.) 9 December 1980 see column 4, line 47 - column 6, line 40	13,14, 17,18
Y	see figure	3-5
X	WO,A,85 04999 (HARRIS CORP.) 7 November 1985 see page 8, line 2 - page 10, line 4	13,14, 17,18
Y	see figure 2	3-5

3

INTERNATIONAL SEARCH REPORT

International application No.
PCT/GB96/00947

Box I Observations where certain claims were found unsearchable (Continuation of item 1 of first sheet)

This international search report has not been established in respect of certain claims under Article 17(2)(a) for the following reasons:

1. ☐ Claims Nos.:
because they relate to subject matter not required to be searched by this Authority, namely:

2. ☐ Claims Nos.:
because they relate to parts of the international application that do not comply with the prescribed requirements to such an extent that no meaningful international search can be carried out, specifically:

3. ☐ Claims Nos.:
because they are dependent claims and are not drafted in accordance with the second and third sentences of Rule 6.4(a).

Box II Observations where unity of invention is lacking (Continuation of item 2 of first sheet)

This International Searching Authority found multiple inventions in this international application, as follows:

see continuation sheet

1. ☒ As all required additional search fees were timely paid by the applicant, this international search report covers all searchable claims.

2. ☐ As all searchable claims could be searches without effort justifying an additional fee, this Authority did not invite payment of any additional fee.

3. ☐ As only some of the required additional search fees were timely paid by the applicant, this international search report covers only those claims for which fees were paid, specifically claims Nos.:

4. ☐ No required additional search fees were timely paid by the applicant. Consequently, this international search report is restricted to the invention first mentioned in the claims; it is covered by claims Nos.:

Remark on Protest

☐ The additional search fees were accompanied by the applicant's protest.

☒ No protest accompanied the payment of additional search fees.

FURTHER INFORMATION CONTINUED FROM PCT/ISA/210

Group I: Claims 1-12;
Group II: Claims 13-19.

Group I: Adaptive filter means (filtering step), whose coefficients in a time slot are used as initial values in adaptive filtering the data received in the corresponding time slot of the next frame.

Group II: Correlation means, for determining the carrier phase at a predetermined symbol in a received data packet.

INTERNATIONAL SEARCH REPORT

Information on patent family members

International Application No
PCT/GB 96/00947

Patent document cited in search report	Publication date	Patent family member(s)		Publication date
EP-A-0106136	25-04-84	US-A-	4475211	02-10-84
		CA-A-	1194139	24-09-85
		JP-A-	59070027	20-04-84
EP-A-0639914	22-02-95	US-A-	5425058	13-06-95
		CA-A-	2124491	29-01-95
		JP-A-	7154436	16-06-95
US-A-4583048	15-04-86	NONE		
US-A-4238739	09-12-80	NONE		
WO-A-8504999	07-11-85	US-A-	4599732	08-07-86
		CA-A-	1246152	06-12-88
		DE-T-	3590158	26-06-86
		EP-A-	0186691	09-07-86
		GB-A,B	2170978	13-08-86